REMARKS

Attached hereto is a marked-up version of the changes made by the current amendment captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**"

Claims 1 – 14 and 16 remain in the application, claim 15 having been cancelled and the subject matter thereof incorporated into its parent claim 14.

Claims 1-16 have been rejected under 35 USC 103(a) as unpatentable over Lin et al in view of Fontana and Sethi. Lin et al discloses a method for forming a split-gate flash memory cell having reduced size, increased coupling ratio and improved program speed. A split-gate cell is provided wherein the a polysilicon layer forms a floating gate disposed over an intervening intergate oxide formed over a second polysilicon layer forming the control gate. The second polysilicon layer is also formed over the source region and overlying the other otherwise exposed portion of the floating gate such that the additional poly line shares the voltage between the source and the floating gate, thereby reducing punch-through and junction breakdown voltages. To the extent that this disclosure is relevant to the present invention it is substantially identical to the prior art device described in the present application and fails to disclose or even suggest Applicant's novel method of providing increased coupling ratio by initially forming a central source region that extends substantially further across what is to be the device channel before the gate electrodes are formed.

Both Fontana and Sethi relate to improvements in FLOTOX technology in which inter alia different gate oxide thicknesses including a thinned portion of the gate oxide formed over the preformed drain region are used to improve operational characteristics of the devices. Neither of these references disclose or suggest Applicant's invention as claimed, or suggest how the teaching of Lin et al might be modified to result in the claimed invention.

More specifically, none of the references disclose or even suggest implanting additional ions into portions of a substrate defined by first and second floating gate regions, and including opposite extremities of a common source region, in order to adjust the threshold voltage of the

flash memory device as recited in Applicant's claims. Applicant therefore respectfully submits that the claims as presently presented clearly define over the the references taken either singly or collectively and reconsideration of the rejection is requested.

Having thus amended the application as suggested by the Examiner, and having amended the claims to more clearly recite Applicant's invention, it is respectfully submitted that the application is in condition for allowance, and early notice thereof is solicited. Should further amendment be deemed necessary prior to allowance, the Examiner is respectfully invited to contact the undersigned by telephone at the number set out below.

Date: 10/9/02

Respectfully submitted,

Claude A.S. Hamrick
Reg. No. 22,586

OPPENHEIMER WOLFF & DONNELLY LLP
Customer No. 25696
P.O. Box 10356
1400 Page Mill Road
Palo Alto, CA 94303
Tel: (650) 320-4000
Fax: (650) 320-4100

CERTIFICATE OF MAILING (37 CFR 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited on October 9, 2002, with the U.S. Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C., 20231.

Date: October 9, 2002

Vicki Naso

"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

IN THE CLAIMS

Please amend the claims as follows:

1. (Once amended) A method of fabricating a flash memory device including an array of split gate cells, comprising the steps of:

providing a silicon substrate having a top surface;

forming a common source region in an area of said top surface for each said cell;

implanting ions into [a] predefined areas [of said substrate to form] on opposite sides of each said common source region [of said substrate];

forming [at least one] a pair of floating gates [over said substrate, each said floating gate being] associated with [one of] each said cell[s and], each said floating gate having a substantial portion thereof overlying one of said predefined areas [which overlies a portion of said common source region, the overlying portion of each floating gate providing for a high coupling ratio for the associated flash cell];

forming [a] select gates each having a first extremity extending over at least a portion of [each] one of said floating gates; and

forming a pair of drain regions associated with each said cell, each said drain region being positioned proximate a second extremity of one of said select gates;

whereby said step of implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell.

2. (Once amended) A method of fabricating a flash memory device as recited in claim 1, wherein said step of [implanting] forming a common source region on said substrate includes the steps of[:]

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting [said] ions into said substrate to form said common source region [of said substrate] using said patterned photoresist as an implant mask; and

removing said patterned photoresist.

3. (Once amended) A method of fabricating a flash memory device as recited in claim 2, wherein said ions implanted to form said common source region include arsenic ions.

4. (Once amended) A method of fabricating a flash memory device as recited in claim 1, wherein said step of [implanting ions into a] forming a common source region [of said substrate] includes the steps of[:]

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting [said] ions into said substrate to form said common source region [of said substrate] using said patterned photoresist as an implant mask; and

removing said patterned photoresist and said sacrificial oxide layer.

5. (Once amended) A method of fabricating a flash memory device as recited in claim 1, wherein said step of implanting ions [forming at least one floating gate over said substrate] includes the steps of[:]

forming a tunneling oxide layer over [the exposed] each said top surface area of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose [at least one] first and second portions [and at least one second portion] of said first polysilicon layer, said exposed first and second [exposed] portions substantially defining first and second floating gate regions; and

implanting ions into said first and second floating gate regions to adjust said threshold voltage; and

wherein the forming of said pair of floating gates includes the steps of

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide layer disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, [each] said remaining portions of said first polysilicon layer forming [one of said] first and second floating gates associated with each said cell, said floating gates [and] having side walls and [also having] a portion which overlies a portion of said common source region thereby providing a high coupling ratio for [an] the associated cell.

6. (Once amended) A method of fabricating a flash memory device as recited in claim 5, wherein said step of forming [at least one] said select gates [over at least a portion of said floating gate] includes the steps of[:]

forming an insulating layer over [said] the exposed portion of said substrate[, over] and [said] the floating gate oxide layer[, and over] covering said floating gates;

forming a second polysilicon layer over said insulating layer;

forming a conductive layer over said second polysilicon layer; and

removing portions of said conductive layer, said second polysilicon layer, and said insulating layer to form [a plurality of] said select gates [each having a portion overlying a portion of an associated one of said floating gates].

7. (Once amended) A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming an insulating layer over said exposed portion of said substrate[, over] and said floating gate oxide layer[, and over] covering said floating gates includes the steps of[:]

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates; and

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer.

8. (Not amended) A method of fabricating a flash memory device as recited in claim 6, wherein said conductive layer includes tungsten.

9. (Not amended) A method of fabricating a flash memory device as recited in claim 1, wherein said ions includes Boron ions.

10. (Once amended) A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming [a] drain regions associated with each cell includes the steps of[:]

patterning and etching said conductive layer and portions of said substrate to substantially define the boundaries of [at least one] drain areas of said substrate; and

implanting ions into said drain areas [of said substrate] to form [at least one] said drain regions.

11. (Once amended) A method of fabricating a flash memory device as recited in claim 4, wherein said step of implanting said ions into said substrate to form said common source region [of said substrate using said patterned photoresist as an implant mask] includes[:]

implanting arsenic ions to provide a dopant density in the range of 1 x 10^{14}/cm2 to 5 x $10^{14}/cm^2$ and at an energy range of 80 to 150 KeV.

12. (Once amended) A method of fabricating a flash memory device as recited in claim 5, wherein said step of depositing a first polysilicon layer over said tunneling oxide layer includes:

depositing [said first] polysilicon [layer] upon said tunneling at a temperature of approximately 620 degrees C in order to form said first polysilicon layer having a thickness in the range of 500 to 2500 angstroms.

13. (Not amended) A method of fabricating a flash memory device as recited in claim 12, wherein said first polysilicon layer includes SiH4.

14. (Once amended) A method of fabricating a flash memory device having a high coupling ratio, comprising the steps of[:]

providing a silicon substrate having a top surface;

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist layer disposed over said sacrificial oxide layer to substantially define a source region of the substrate;

implanting first ions into said substrate to form a common source region of said substrate using the patterned photoresist layer as an implant mask;

removing said patterned photoresist layer and said sacrificial oxide layer to expose said top surface of said substrate;

forming a tunneling oxide layer over the exposed top surface of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose at least one first portion and at least one second portion of said first polysilicon layer, said first and second exposed portions substantially defining first and second floating gate regions;

implanting second ions into portions of said substrate defined by said first and second floating gate regions and including opposite extremities of said common source region, in order to adjust the threshold voltage of the flash memory device;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide layer disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, each said remaining portion of said first polysilicon layer forming a floating gate [associated with a cell and] having side walls, [and also] having a portion which overlies a portion of said common source region there by providing a high coupling ratio for an associated cell;

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates;

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer

forming a second polysilicon layer over said second gate oxide layer;

forming a conductive layer over said second polysilicon layer;

removing portions of said conductive layer, said second polysilicon layer, said second gate oxide layer, said nitride spacers and said first gate oxide layer to form a plurality of select gates each having a portion overlying a portion of an associated one of said floating gates; and

patterning and etching said conductive layer to expose portions of said substrate to substantially define the boundaries of at least one drain area of said substrate; and

implanting [second] third ions into said drain area of said substrate to form at least one drain region.

Cancel claim 15 without prejudice.

16. (Once amended) A method of fabricating a flash memory device as recited in claim [15] 14, wherein said first ions include N-type ions and said additional ions include P-type ions, whereby threshold voltage[s] of the flash memory [cells are] device is adjusted.